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EFFECT OF ANNEALING TEMPERATURE ON THE SURFACE MORPHOLOGY AND ELECTRICAL PROPERTIES OF SnO_2 THIN FILMS

Madraximov Mo’minjon Mo’ydinovich.
Tuychibayev Baxodir Kurbonaliyevich
Fergana State Technical University

Abstract

This paper presents a structured analysis of the effect of annealing temperature on the surface morphology and electrical behavior of SnO_2 thin films on the basis of scanning electron microscopy observations and semiconductor transport considerations. The results show that, as the annealing temperature increases, the film surface evolves from a relatively porous and weakly crystallized nanostructure toward a dense polycrystalline morphology with larger and more clearly faceted grains. Such evolution is associated with thermally activated atomic diffusion, progressive grain coalescence, and a reduction in the Gibbs free energy of the system. At lower temperatures, the limited mobility of adatoms preserves a high density of grain boundaries and intergranular voids, which enhances potential barriers and suppresses charge transport. At higher temperatures, grain growth and densification reduce the boundary fraction, weaken carrier scattering, and create more continuous conductive pathways. The analysis confirms that annealing temperature is a decisive technological parameter for tailoring the structural quality and functional performance of SnO_2 thin films for semiconductor and optoelectronic applications.

Keywords

SnO_2 thin films; annealing temperature; scanning electron microscopy; grain growth; grain boundary barriers; electrical conductivity; polycrystalline semiconductor.

1. Introduction

Tin dioxide (SnO_2) is a wide-band-gap n-type oxide semiconductor that is extensively employed in gas sensors, transparent conducting layers, optoelectronic elements, and other thin-film devices. The practical behavior of this material is governed not only by its intrinsic band structure but also by the microstructural state of the deposited layer, including crystallite size, grain-boundary density, surface defect concentration, and oxygen-related vacancy states. For this reason, post-deposition thermal treatment is one of the most important technological tools for controlling the structure and functionality of SnO_2 thin films.

The source material used for this article focuses on SEM-based morphological analysis and provides a physically grounded interpretation of how annealing temperature modifies the grain ensemble and, consequently, the expected transport behavior of the layer. In a polycrystalline oxide semiconductor, the morphology of the surface is directly connected with the density of electrically active intergranular regions. Therefore, the interpretation of SEM data is not limited to descriptive imaging but also provides insight into charge transport, grain-boundary barrier formation, and the evolution of conductive channels within the film.

The aim of the present article is to reorganize the provided text into a journal-style discussion suitable for a Scopus-oriented manuscript format. Particular attention is given to the sequence of morphological transformations observed with increasing annealing temperature and to their connection with diffusion kinetics, grain growth mechanisms, and electrically relevant boundary effects.

2. Morphological Background and Transport Considerations

The influence of annealing temperature on the morphology of a thin film is primarily governed by thermally activated diffusion. As the temperature rises, surface and bulk atoms acquire sufficient energy to migrate toward energetically more favorable lattice positions. This process promotes structural ordering, crystal growth, and densification of the film. In the simplest form, the diffusion coefficient is described by the Arrhenius relation:

$$D = D_0 \exp(-E_a / kT)$$

where D is the diffusion coefficient, D_0 is the pre-exponential factor, E_a is the activation energy of diffusion, k is the Boltzmann constant, and T is the absolute temperature. When T is low, D remains small and the relocation of atoms is limited; as a result, incomplete crystallization, fine-grained morphology, and a high concentration of intergranular voids are preserved.

For polycrystalline semiconductors, grain boundaries often play the role of electrically active barriers. Localized states, adsorbed oxygen species, and charged defects may accumulate in boundary regions, which gives rise to intergranular potential barriers and suppresses free-carrier transport. In this regime, the conductivity can be qualitatively interpreted using the Seto-type relationship:

$$\sigma = \sigma_0 \exp(-q\varphi\_b / kT)$$

where σ is the electrical conductivity, σ_0 is a material-dependent constant, q is the elementary charge, and φ_b is the grain-boundary potential barrier height. Thus, the microstructure observed by SEM is directly relevant to the expected electrical response: a fine-grained, porous film with many boundaries should exhibit lower conductivity than a dense film with larger grains and a reduced boundary fraction.

When annealing becomes sufficiently intense, grain growth and grain coalescence reduce the number of intergranular barriers. In that case, the conductivity tends to improve due to an increase in carrier mobility, which can be expressed in the usual transport form:

$$\sigma = qn\mu$$

where n is the carrier concentration and μ is the carrier mobility. The enlargement of grains and the reduction of scattering centers increase μ, while the formation of more continuous current pathways enhances macroscopic transport through the layer.

3. Results and Discussion

The SEM observations reveal a regular and physically meaningful evolution of the SnO_2 thin-film surface as the annealing temperature increases. In general, the morphology changes from a relatively loose nanocrystalline arrangement toward a compact polycrystalline structure with larger and better defined grains. This transition reflects the gradual predominance of thermally activated diffusion, the merging of neighboring grains, and the tendency of the system to reduce its surface and grain-boundary energy.

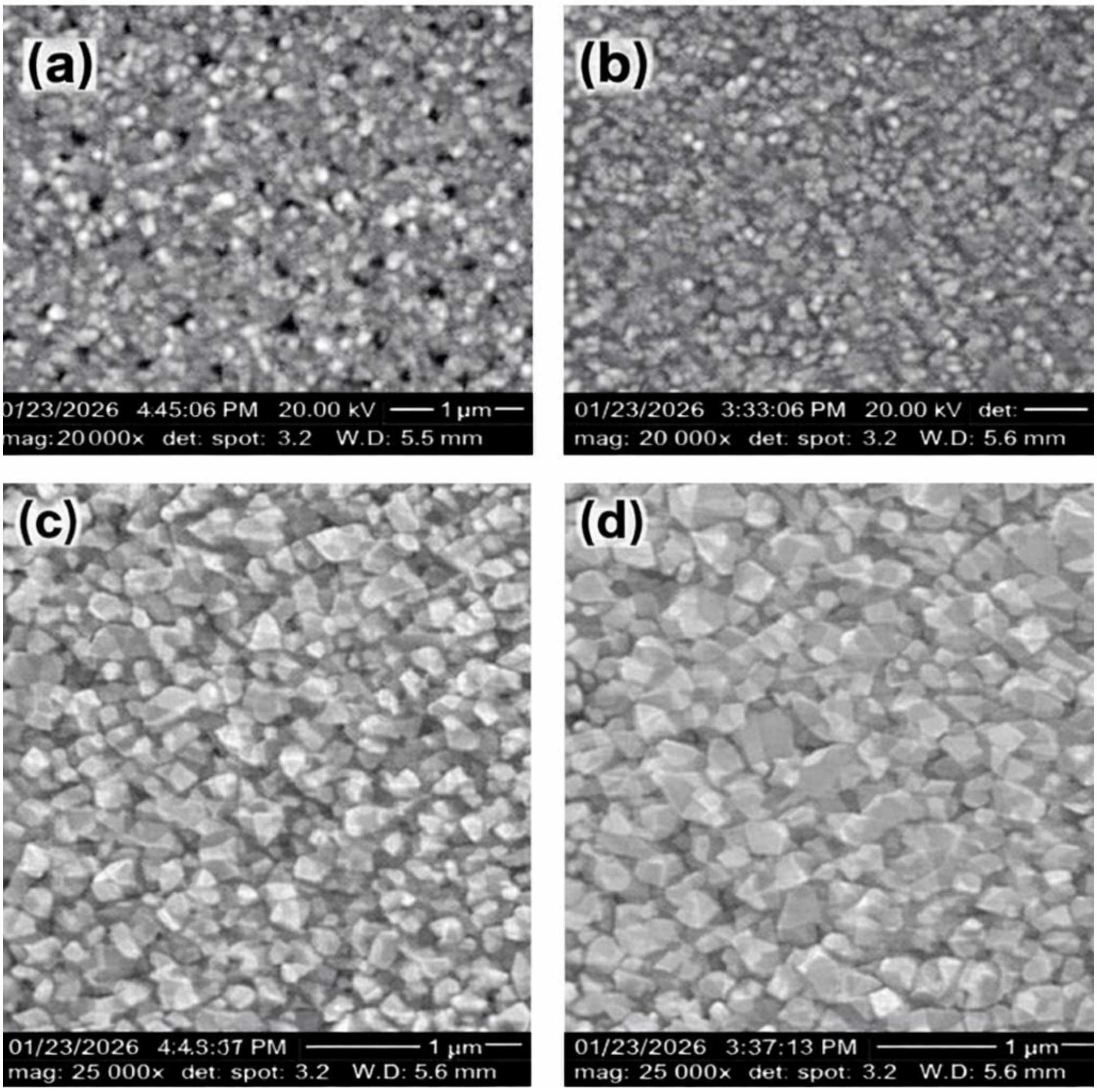

Figure 1. SEM micrographs of SnO_2 thin films annealed at different temperatures: (a) low-temperature regime with fine porous grains; (b) initial densification and improved packing; (c) pronounced grain growth with polygonal crystallites; and (d) compact high-temperature morphology with larger grains and reduced porosity.

As shown in Figure 1(a), the film treated at the lowest annealing temperature is characterized by small grains, weakly expressed grain contours, relatively loose packing, and a large number of intergranular boundaries. Such a morphology indicates that the thermal energy supplied to the system is insufficient for extensive atom migration and structural rearrangement. Consequently, the crystallization process remains incomplete, and the surface preserves a highly dispersed nanocrystalline character. From the standpoint of semiconductor transport, this type of morphology is unfavorable because the large fraction of boundaries increases the probability of carrier trapping and barrier-controlled conduction.

The micrograph in Figure 1(b) represents an intermediate stage of evolution in which the surface becomes more homogeneous, the grains are packed more closely, and the continuity of the film improves. This transition suggests that annealing has already activated a noticeable level of diffusion, allowing atoms to occupy more stable positions and reducing the number of metastable configurations. Although grain nucleation effects are still present, the onset of boundary rearrangement and local densification can be clearly inferred from the reduction of open gaps between neighboring grains.

A more pronounced structural transformation is visible in Figure 1(c), where substantial grain enlargement and the appearance of distinctly faceted polygonal crystallites are observed. At this stage, the dominant mechanism shifts from predominantly nucleation-limited behavior to grain-growth-driven evolution. The decrease in void space and the emergence of better defined grain shapes indicate that the system is minimizing its interfacial energy through coalescence and competitive growth of larger crystallites at the expense of smaller ones. This process is of major electrical importance because a lower grain-boundary density reduces carrier scattering and decreases the effective barrier network that impedes transport.

The highest-temperature specimen, shown in Figure 1(d), exhibits the most compact and structurally developed morphology. The grains are larger, the interfaces are more clearly formed, and the overall film appears denser than in the preceding states. In an n-type oxide such as SnO_2, adsorbed oxygen and charged defect states at the surface or at grain boundaries can withdraw electrons and generate depletion regions. When the grains are very small, these depleted zones may occupy a significant fraction of the entire grain volume, strongly suppressing conductivity. By contrast, when the grains become larger, only the near-surface part is substantially depleted, while the grain interior preserves a comparatively freer conduction path. The high-temperature morphology is therefore expected to support more efficient electron transport.

Taken together, the SEM results indicate that increasing annealing temperature produces a step-by-step transition from a weakly crystallized and relatively porous nanostructure to a dense, well-developed polycrystalline film. The main driving forces behind this evolution are thermally activated diffusion, grain coalescence, preferential growth of larger grains, and the overall reduction of Gibbs free energy. The corresponding decrease in the boundary fraction leads to less carrier scattering, lower intergranular barrier influence, and the formation of more continuous conducting channels. Hence, annealing temperature should be regarded as a key technological parameter for simultaneous control of morphology, crystallinity, defect-related boundary states, and the electrical-functional behavior of SnO_2 thin films.

4. Conclusion

The journal-style analysis prepared from the provided source text demonstrates that the morphology of SnO_2 thin films is highly sensitive to annealing temperature. Low-temperature treatment preserves a fine-grained and porous structure with many electrically active boundaries, whereas higher-temperature annealing promotes densification, grain growth, and the development of a more continuous polycrystalline network. This morphological evolution is explained by thermally activated diffusion, intergranular merging, competitive grain growth, and free-energy minimization. Because the reduction of grain-boundary density facilitates carrier transport, the structural changes observed by SEM are expected to translate into improved electrical conductivity. Accordingly, annealing temperature is identified as one of the most important technological parameters for optimizing SnO_2 thin films intended for semiconductor and optoelectronic applications.

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